JPL

FLIGHT ARRAY PROCESSOR

I. INTRODUCTION

II. SPACEFLIGHT APPLICATIONS FOR ARRAY PROCESSORS

III. DESIGN CONSIDERATIONS FOR FLIGHT ARRAY PROCESSORS

IV. ISSUES REGARDING SPACEFLIGHT APPLICATIONS OF ARRAY PROCESSORS

WJR-4/17/85

P-10

JPL

INTRODUCTION

- OBJECTIVES
  - DEVELOP AN ADVANCED HIGH SPEED ARRAY PROCESSOR FOR SPACE STATION USE.
  - MAKE SCIENTIFIC AND ENGINEERING INFORMATION AVAILABLE IN REAL TIME (OR FOR LATER USE).
  - ENABLE MORE EFFECTIVE USE OF DOWNLINK AND INTERSPACECRAFT COMMUNICATIONS, E.G., DATA COMPRESSION AND ENCODING.
  - MAKE DATA AND SIGNAL PROCESSING SOFTWARE EASIER TO DESIGN AND CODE AS WELL AS MORE RELIABLE.

WJR-4/17/85

JPL

SPACEFLIGHT APPLICATIONS FOR ARRAY PROCESSORS

- APPROACH
  - USE AS BASELINE, TWO EXISTING PROGRAMS: NSCAT AND ADSP.
    - NSCAT - NASA SCATTEROMETER. FLOWN AS PART OF NAVY REMOTE OCEAN SENSING SYSTEM (NROSS). MEASURE OCEAN SURFACE WINDS.
    - ADSP - ADVANCED DIGITAL SAR PROCESSOR. GROUND-BASED EQUIPMENT BEING DEVELOPED BY JPL FOR PROCESSING SPACECRAFT EARTH OBSERVATIONS.

WJR-4/17/85

DESIGN CONSIDERATIONS FOR FLIGHT ARRAY PROCESSORS

JPL

- NSCAT (FIGURE 1) - STUDY CONTRACT WITH STANFORD UNIVERSITY.
  - WIND MEASUREMENT RADAR (SCATTEROMETER);
  - ESTIMATE SURFACE WIND VELOCITY OVER OCEAN;
    - OBSERVE VARIATION OF OCEAN RADAR CROSS SECTION USING ANGLE OF INCIDENCE, POLARIZATION AND LOOK DIRECTION.
  - PROCESSING REQUIREMENTS: PERFORM EIGHT-256 POINT FOURIER TRANSFORMS DURING 17 MILLISECONDS BETWEEN RADAR PULSES. 16 BIT ACCURACY, 8 BIT DATA SAMPLES.
- ARRAY PROCESSOR FOR NSCAT (FIGURE 2)
  - MODEST PROCESSING REQUIREMENT: 256 POINT FFT, 400 NS/BUTTERFLY.

$$(8 \text{ PASSES})\left(\frac{256}{2} \times \frac{\text{BUTTERFLIES}}{\text{PASS}}\right)\left(400\ \frac{\text{NS}}{\text{BUTTERFLY}}\right) \cong .4\text{MS FOR ONE 256 POINT FFT.}$$

8 - 256 POINT FFT: (8) (.4MS) $\cong$ 3.2 MS VS AVAILABLE 17MS.

- INCORPORATION OF ALGORITHM IMPROVEMENT:
  - PROGRAMMABLE THEREFORE SOME FLEXIBILITY:
  - ABLE TO ACCOMMODATE CHANGES, E.G., ALGORITHM IMPROVEMENTS, MORE READILY.
  - ALLOWS FOR CALCULATION OF NEW SIGNAL STATISTICS NOT CURRENTLY REQUIRED FOR WIND MEASUREMENTS. EXAMPLE IS QUANTITIES WHICH CAN BE CALCULATED FROM RAW RADAR ECHO DATA, BUT WHICH COULD NOT BE CALCULATED FROM THE AVERAGED DATA THAT IS DOWNLINKED.

WJR-4/17/85

PRELIMINARY BASELINE NROSS SCATTEROMETER FUNCTIONAL BLOCK DIAGRAM

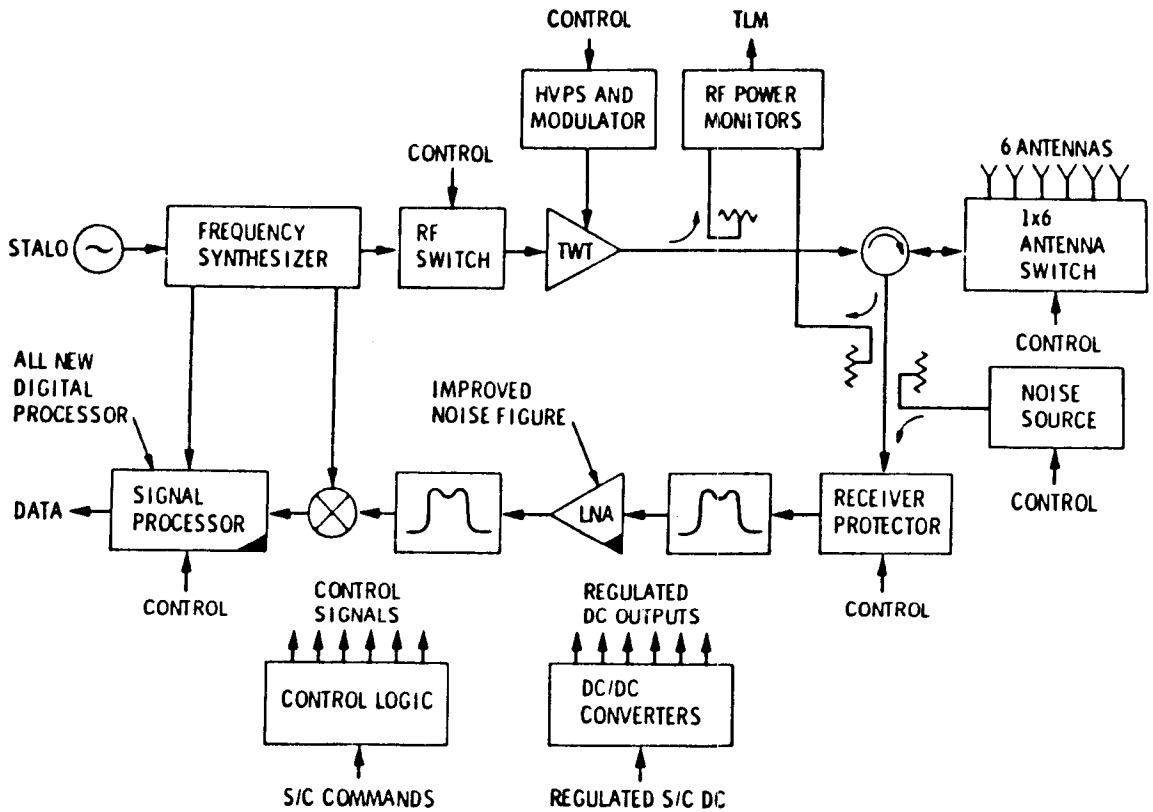

Figure 1. Functional block diagram for the NROSS wind measurement radar called NSCAT. The item discussed here is the signal processor at lower left.

WJR-4/17/85

MP - AP SIGNAL PROCESSOR CONCEPT FOR NSCAT

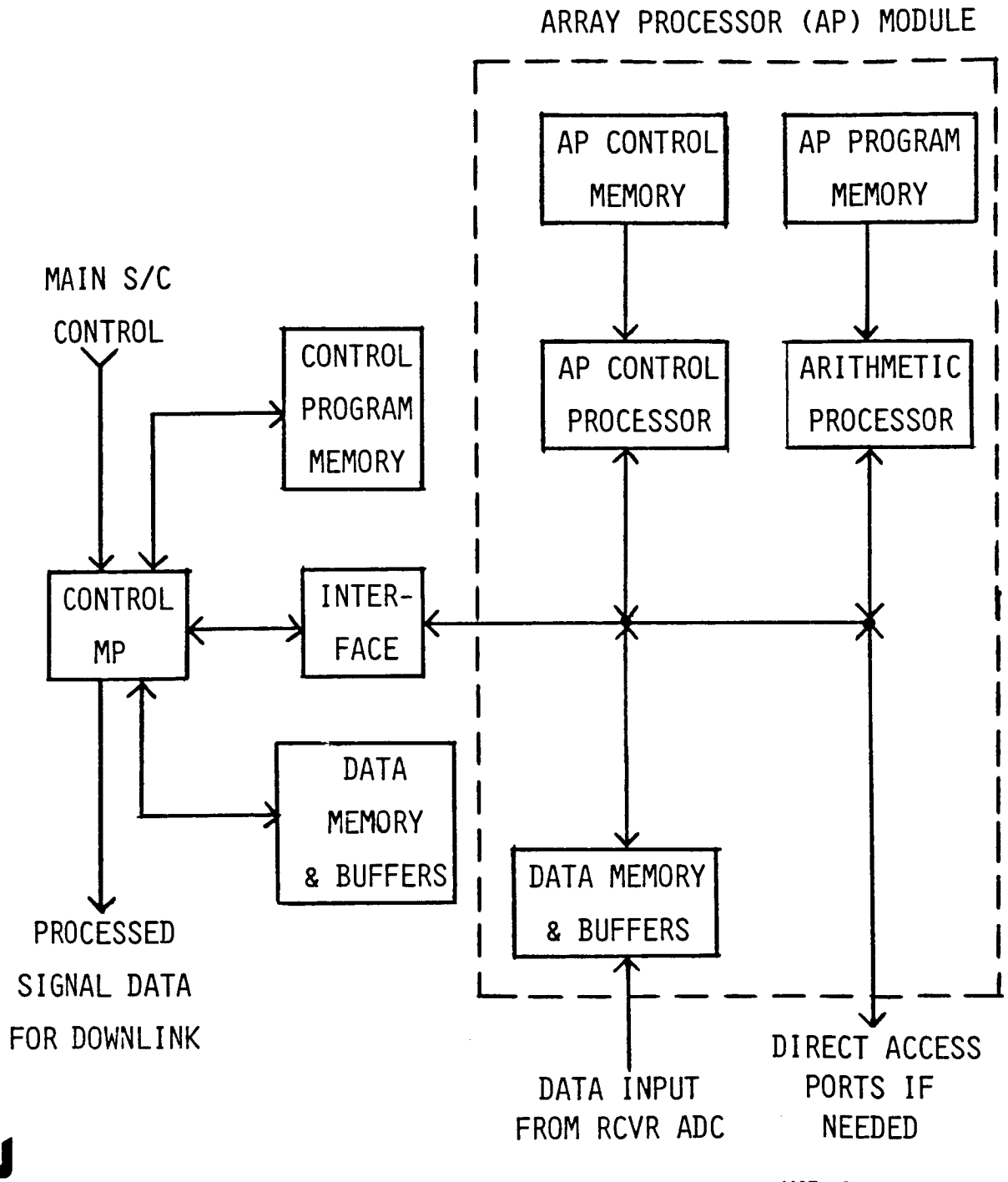

FIGURE 2. MICROPROCESSOR - ARRAY PROCESSOR (MP-AP) CONCEPT FOR THE NROSS WIND MEASUREMENT RADAR (NSCAT) SIGNAL PROCESSOR.

WJR-4/17/85

JPL

DESIGN CONSIDERATION FOR FLIGHT ARRAY PROCESSORS

- ADSP (FIGURE 3) - STUDY CONTRACT WITH UNIVERSITY OF ARIZONA
  - EARTH OBSERVATION
  - PROCESSING REQUIREMENT (SIR-B AS BASELINE): APPROXIMATELY 1.5 GIGAFLOPS.
  - WESTINGHOUSE VSHIC COMPLEX ARITHMETIC VECTOR PROCESSOR CAPABLE OF 40 MILLION COMPLEX FFT BUTTERFLIES/SEC. (40 MCOPS).
  - 40 MCOPSX 10 $\frac{\text{FLOP}}{\text{BUTTERFLY}}$ = .4 GIGAFLOPS. LESS THAN 50 WATTS.
  - HUGE RAM - 160 MBYTES.
  - BLOCK OUT DESIGN.
  - POWER, WEIGHT, VOLUME, RADIATION HARDNESS, SEU.
  - KNOWING BOUNDS, HOW FEASIBLE IS IT?

WJR-4/17/85

ADSP STATUS REPORT
HARDWARE BLOCK DIAGRAM

JPL

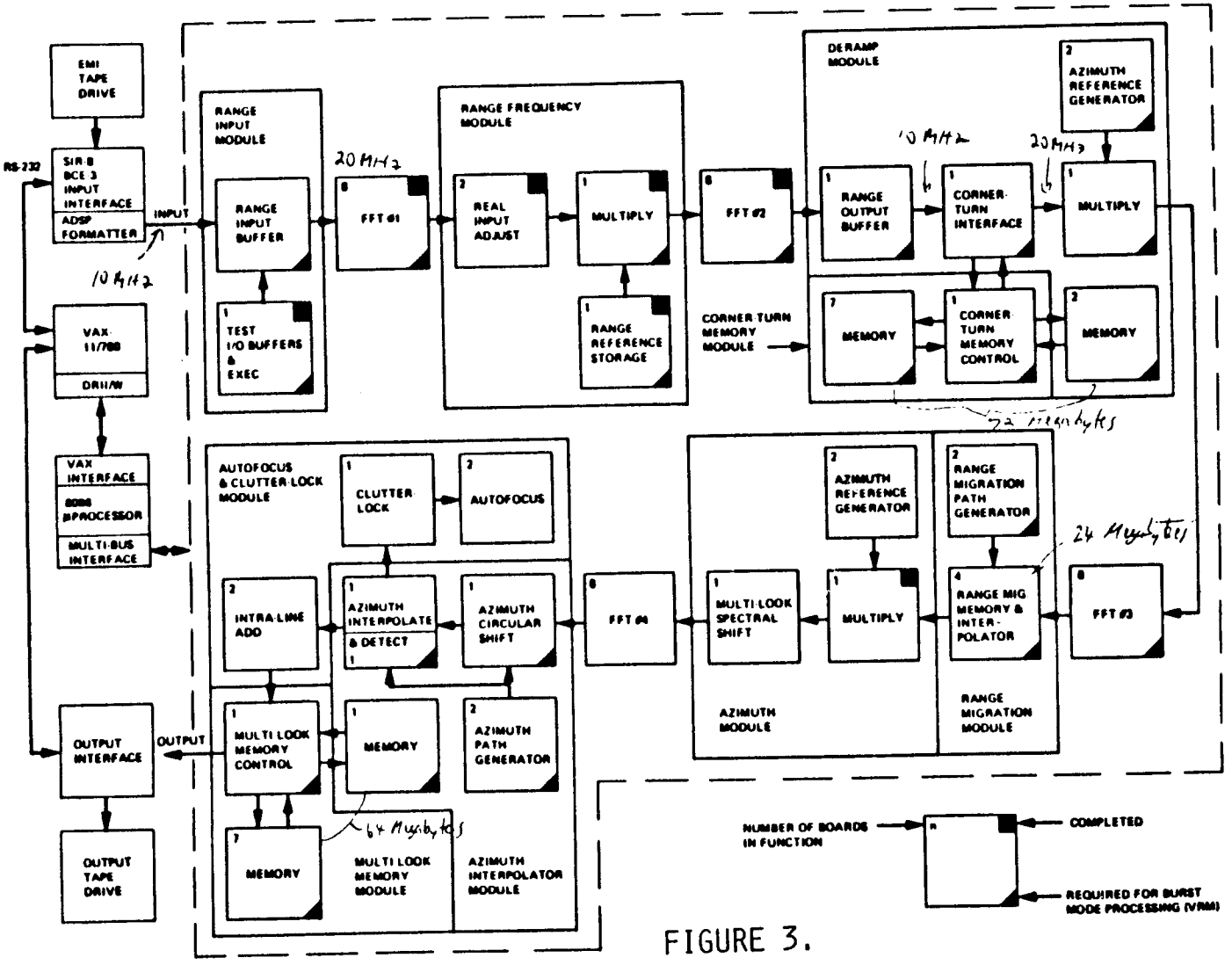

FIGURE 3.

WJR
4/17/85

ORIGINAL PAGE IS
OF POOR QUALITY

ISSUES REGARDING SPACEFLIGHT APPLICATIONS OF ARRAY PROCESSORS

JPL

- TRANSMISSION TO EARTH OF RAW VS. SPACECRAFT PROCESSED DATA.
  - IF LARGE AMOUNTS OF DATA (E.G., IMAGES OF THE EARTH) CAN BE COMPRESSED (FILTERED), COMMUNICATION COSTS ARE LOWERED. BUT CAN THE COMPRESSED DATA SATISFY THE USER?
- NEED FOR REAL TIME SIGNAL AND IMAGE PROCESSING ONBOARD SPACECRAFT.
  - SPACE STATION - CREW MEMBERS WOULD NEED REAL TIME SOLAR IMAGES TO ACTIVATE SOLAR FLARE OBSERVATIONS AS OCCURRED DURING SKYLAB. DOES CREW NEED REAL TIME INFORMATION TO CONTROL EXPERIMENTS AND OBSERVATIONS OR WILL THE CONTROL FUNCTION BE DONE ON GROUND VIA SPACECRAFT CONTROL CENTER (SPOCC)? IF THE CREW PLAYS AN IMPORTANT OR EXCLUSIVE ROLE, THEN SPACECRAFT ARRAY PROCESSORS COULD PLAY A VERY SIGNIFICANT ROLE IN PROVIDING NECESSARY REAL TIME DATA.
- COMPATIBLE BUS SPEEDS
  - EASY TO SEE A SEVERE BOTTLENECK WOULD DEVELOP IF A FAST ARRAY PROCESSOR INTERFACED TO A SPACECRAFT SYSTEM WITH INSUFFICIENT SPEED TO PROVIDE DATA TO OR ACCEPT OUTPUT FROM AN ARRAY PROCESSOR.
  - WORKING CLOSELY WITH JPL'S MAX HIGH SPEED COMPUTER DESIGN GROUP (I.E., MAX COULD BE THE HOST FOR THE ARRAY PROCESSOR). WJR-4/17/85

JPL

ISSUES REGARDING SPACEFLIGHT APPLICATIONS OF ARRAY PROCESSORS

(CONTINUED)

- TECHNOLOGY
  - VHSIC
  - SANDIA 32000
  - GaAs
  - OTHER

WJR-4/17/85